## CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method for controlling data transfer between embedded resources in a device using middleware, comprising the steps of:

separating a functionality of said middleware into a control interface and a data interface, said middleware functionality enabling interoperability of said device with other devices in a given system, said other devices also using said middleware to provide said functionality, said middleware functionality also enabling a software object resident on a general purpose processor of said device to transfer data between said embedded resources, there being a control interface and a data interface for each of said object and each of said embedded resources;

constructing said control interfaces within said general purpose processor of said device;

extracting said data interfaces for said embedded resources outside said general purpose processor, such that said data transfer, under control of said object exercised through said middleware via said control interfaces, occurs directly between said embedded resources without going through said general purpose processor.

2. A method as in claim 1, wherein said respective control interfaces for each of said embedded

resources are implemented using device drivers of said respective embedded resources.

3. A method as in claim 1, wherein said respective data interfaces for each of said embedded resources are each connected to a switch matrix, said switch matrix being external to said general purpose processor and serving to connect said embedded resources.

4. A method as in claim 3, wherein said switch matrix is implemented as a connection fabric.

5. A method as in claim 3, wherein said switch matrix is implemented as a shared memory.

6. A method as in claim 1, wherein said device is a software defined radio, said given system is the Joint Tactical Radio System, and said middleware is compliant with Software Communications Architecture (SCA).

7. A method as in claim 3, wherein one of said embedded resources is a Field Programmable Gate Array (FPGA).

8. A method as in claim 7, further comprising the steps of:

creating an Interface Description Language (IDL) description of a raw interface of said FPGA;

generating from said IDL a description of an interface between a core functionality of said FPGA and said switch matrix, and a description of a

controller for performing said core functionality; and

integrating said core functionality interface into said data interface of said FPGA, and integrating said controller into said control interface of said FPGA.

9. A system for controlling data transfer between embedded resources in a device using middleware, comprising:

means for separating a functionality of said middleware into a control interface and a data interface, said middleware functionality enabling interoperability of said device with other devices in a given system, said other devices also using said middleware to provide said functionality, said middleware functionality also enabling a software object resident on a general purpose processor of said device to transfer data between said embedded resources, there being a control interface and a data interface for each of said object and each of said embedded resources;

means for constructing said control interfaces within said general purpose processor of said device;

means for extracting said data interfaces for said embedded resources outside said general purpose processor, such that said data transfer, under control of said object exercised through said middleware via said control interfaces, occurs directly between said embedded resources without going through said general purpose processor.

10. A system as in claim 9, wherein said respective control interfaces for each of said embedded resources are implemented using device drivers of said respective embedded resources.

11. A system as in claim 9, wherein said respective data interfaces for each of said embedded resources are each connected to a switch matrix, said switch matrix being external to said general purpose processor and serving to connect said embedded resources.

12. A system as in claim 11, wherein said switch matrix is implemented as a connection fabric.

13. A system as in claim 11, wherein said switch matrix is implemented as a shared memory.

14. A system as in claim 9, wherein said device is a software defined radio, said given system is the Joint Tactical Radio System, and said middleware is compliant with Software Communications Architecture (SCA).

15. A system as in claim 11, wherein one of said embedded resources is a Field Programmable Gate Array (FPGA).

16. A system as in claim 15, further comprising:

means for creating an Interface Description Language (IDL) description of a raw interface of said FPGA;

means for generating from said IDL a description of an interface between a core functionality of said FPGA and said switch matrix, and a description of a controller for performing said core functionality; and

means for integrating said core functionality interface into said data interface of said FPGA, and integrating said controller into said control interface of said FPGA.